AMENDMENTS TO THE CLAIMS

1. (Original) A network storage apparatus for connecting a host computer with at least one storage device, comprising:

a passive backplane having a plurality of data buses including first and second data buses;

at least first and second channel interface modules, connected to said passive backplane and adapted to be connected to the host computer and the at least one storage device, that are operational to send and receive storage data to and from the host computer and the at least one storage device and that are operational to selectively transfer the storage data to one or more of said plurality of data buses; and

at least first and second controller memory modules, connected to said passive backplane, that communicate with said channel interface modules via said passive backplane, and that store and process the storage data transferred to and from said channel interface modules;

wherein at least said first controller memory module includes a direct memory access (DMA) engine and said DMA engine is used in transferring data between said first controller memory module and said second controller memory module.

2. (Original) The apparatus of Claim 1, wherein:

at least said first channel interface module includes a communication path portion and a channel interface portion, wherein said channel interface portion is operable to transfer the storage data between the host computer and/or the at least one storage device and said communication path portion, and said communication path portion is operational to selectively transfer the storage data between said channel interface portion and said passive backplane.

3. (Original) The apparatus of Claim 1, wherein:

at least said first controller memory module includes a bus interface portion that connects to said passive backplane, a memory for temporary storage of said storage data, and a processing portion that organizes and arranges said storage data.

4. (Original) The apparatus of Claim 3, wherein said bus interface portion includes:

at least one backplane interface that connects to said passive backplane;

a memory interface that connects to said memory;

a processing interface that connects to said processing portion;

a bridge core that contains control logic operable to connect said processing interface, memory interface and backplane interface; and

an exclusive OR (XOR) engine that performs XOR functions on data blocks.

5. (Original) The network storage apparatus of Claim 1, wherein said passive backplane further includes:

third and fourth data buses.

6. (Original) The apparatus of Claim 1, wherein each of said first and second data buses is part of a group of backplane buses and said group includes peripheral component interconnect (PCIX) buses.

7. (Original) The apparatus of Claim 2, wherein:

said passive backplane further includes a third data bus and a fourth data bus;

said first channel interface module includes a first bus port and a second bus port, and said second channel interface module includes a third bus port and a fourth bus port, said first, second, third and fourth bus ports being operable to connect said communication path portion to said passive backplane; and

said first controller memory module includes a first bus interface and a second bus interface, and said second controller memory module includes a third bus interface

and a fourth bus interface, said first, second, third and fourth bus interfaces being operable to connect said controller memory module to said first, second, third and fourth data buses of said passive backplane.

8. (Original) The apparatus of Claim 7, wherein

said first bus port is connected to said first data bus and said second bus port is connected to said third data bus;

said third bus port is connected to said second data bus and said fourth bus port is connected to said fourth data bus;

said first bus interface is connected to said first data bus and said second bus interface is connected to said second data bus; and

said third bus interface is connected to said third data bus and said fourth bus interface is connected to said fourth data bus.

9. (Original) The apparatus of Claim 8, wherein:

said communication path portion of said first channel interface module has a first shared path, a first switched path and a second switched path; and

said communication path portion of said second channel interface module has a second shared path, a third switched path and a fourth switched path and in which:

said first shared path is connected to said first bus port and said second bus port;

said first switched path is connected to said first bus port and said channel interface portion;

said second switched path is connected to said second bus port and said channel interface portion;

said second shared path is connected to said third bus port and said fourth bus port;

said third switched path is connected to said third bus port and said channel interface portion; and

said fourth switched path is connected to said fourth bus port and said channel interface portion; and wherein

said first, second, third and fourth switched paths are operable to enable and disable communications involving said channel interface portion.

10. (Original) The apparatus of Claim 1, wherein:

at least said first channel interface module includes a first shared path and the storage data is transferred between said first controller memory module and said second controller module using said first shared path.

11. (Currently Amended) A method for sharing data between a first controller memory module and a second controller memory module, comprising:

providing a first shared path in a first channel interface module, wherein the shared path has a switchable component for determining which data is to be routed over the shared path;

~~and~~ a direct memory access engine ~~in~~ for each of said first and second controller memory modules; and

transferring first data between said first controller memory module and said second controller memory module using said direct memory access engine for at least one of the first and second controller memory modules, wherein said switchable component provides passage of said first data over ~~using~~ said first shared path between the first and second controller memory modules.

12. (Currently Amended) The method of Claim 11, further comprising:

providing a second shared path in a second channel interface module; and

transferring second data between said first controller memory module and said second controller memory module using each of said direct memory access engines, wherein the second data passes through ~~via~~ said second shared path.

13. (Currently Amended) The method of Claim 11, further comprising:

connecting said first and second channel interface modules and said first and second controller memory modules to a passive backplane, wherein the first data passes through the passive backplane during said step of transferring.

14. (Currently Amended) An apparatus for sharing data between a first controller memory module and a second controller memory module, comprising:

at least a first channel interface module having a first shared path, wherein the shared path has a switchable component, operably associated therewith, for selecting which data is to be routed on the shared path;

a first controller memory module including a first direct memory access engine;

a second controller memory module including a second direct memory access engine; and

a communications interface to permit direct communications between said first and second controller memory modules; wherein data is transferred between said first and second controller memory modules using at least one of said first and second direct memory access engines and the switchable component of said first shared path.

15. (Currently Amended) The apparatus of Claim 14, further including ~~wherein~~:

~~said~~ a second channel interface module ~~has~~ having a second shared path, wherein the second shared path has a second switchable component, operably associated therewith, for determining which data is to be routed over the second shared path;

wherein said second switchable component provides passage of second data over said second shared path between the first and second controller memory modules using each of said first and second direct memory access engines.

16. (Previously Presented) The apparatus of Claim 14, wherein:

said communications interface includes a passive backplane.

17. (Previously Presented) The apparatus of Claim 16, wherein:

said passive backplane includes at least first and second peripheral component interconnect (PCIX) buses.

18. (New) The method of Claim 11, wherein the first shared path transmits the first data between the direct memory access engines of the first and second controller memory modules.

19. (New) The method of Claim 11, further including providing a plurality of data buses, wherein each of said data buses is operably connected between a first one of the direct memory access engines and the first shared path for communicating the first data.

20. (New) The method of Claim 19, further including:

providing a second shared path in a second clannel interface module;

transferring second data between said first controller memory module and said second controller memory module using each of said direct memory access engines, wherein the second data passes through said second shared path;

a second plurality of said data buses, wherein each of the second plurality of said data buses is operably connected between a second one of the direct memory access engines and the second shared path for communicating the second data.

21. (New) The method of Claim 12, wherein the second shared path includes a second switchable component for determining which data is to be routed over the second shared path.

22. (New) The method of Claim 13, wherein the passive backplane includes two data busses for communicating with each of the first and second controller memory modules.